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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,486	03/01/2004	Eliyahou Harari	SNDK.304US1	1878

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EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,486	HARARI, ELIYAHOU	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 07/01/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-37* is/are pending in the application.

4a) Of the above claim(s) *9-14 and 31-37* is/are withdrawn from consideration.

5)☒ Claim(s) *22-30* is/are allowed.

6)☒ Claim(s) *15,16,19 and 21* is/are rejected.

7)☒ Claim(s) *17,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1, 6/1, 6/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **15-20** are present for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

3. Claims **15,16, 19, & 21** are rejected under 35 U.S.C. 102(b) as being anticipated by **Forbes et al (5,963,274).**

Forbes et al (see Fig. 1) shows a non-volatile memory array cell array (105), and Fig. 2 also shows such cell array (105) in detail having a plurality of memory cells (200) running or extending in both rows and column fashion in series or strings of cells as claimed. Fig.3A further teaches the claimed configuration as follows:

- Cells (205Bb and 205AB) make up a string of cells extending in a first direction (Y-direction or vertical plane) across a semiconductor substrate (305);
- Cells (205BA and 205AA) make up another string of cells extending also in a first direction (Y-direction or vertical plane) across a semiconductor substrate (305);
- These cells are also spaced apart from each other in a second direction (X-horizontal) as well;

- The two strings of cell include the floating gates (FG, **325**) capacitively coupled to its corresponding drain/source regions (205BB, 205AB, 205BA, 205AA) making up the claimed "storage elements" for storing cell data;
- The control gate (**XG, 335**), see also col. 6-7 and Figs. 3B & 4, is shown as running along the second direction (X-direction or horizontal plane) and is seen as perpendicular to the first direction (vertical) as shown;
- Figs.3B & 4 further shown in detail how ***each control gate (XG2-XG4) is laid out as adjacently and also capacitively coupled to their associated floating gates (325)*** at each location where both line directions are crossed;
- Fig.3B further shows that ***the control gate (XG) is to be capacitively coupled with its sidewalls of the adjacent storage elements*** with the help of a ***dielectric*** layer/material (**340**, see col.8, line 54) disposed in between the floating gates (325) and the extending control gate (XG) as claimed.

Regarding claim **16**, Fig. 3 also shows that beneath each control gate (XG2-XG4), this dielectric layer (34) also insulated these gates from the underlying substrate, thus inherently creates a potential capacitor effect as well;

Regarding claim **19**, Fig.3B shows that the height of each gloating gate and capacitively coupled control gate is extending above the substrate surface with a distance that is larger than its respective widths;

Regarding claim **21**, each control line is positioned within the spacing between adjacent ones of the floating gates in order to be electrically isolated from one another as well;

4. Other remaining claims contain allowable subject matter over prior arts of record for the following reasons:

- Claims **17** recites the feature of "the control lines extend into trenches formed in the substrate" is not shown nor suggested elsewhere;
- Claim **18** adds "the capacitively coupling is characterized by enhancing the substrate conductivity in response to applied voltages" is also not shown or suggested;
- Claim **20** adds the particular polysilicon material on bottom and top portion of control gates;
- Claim **22** and its corresponding dependent claims **23-30** recites particular use of applied voltages and its effects on the levels of charges being stored and/or programmed at each cell storage element, which are not taught, discussed, or fairly suggested in the arts. The dependent claims also add the manufacturing method that is not seen elsewhere in the arts.

5. Claims **17, 18, & 20** are objected as being dependent upon rejected base claims. Claims **22-30** are allowable over prior arts of record.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
7/14/2005